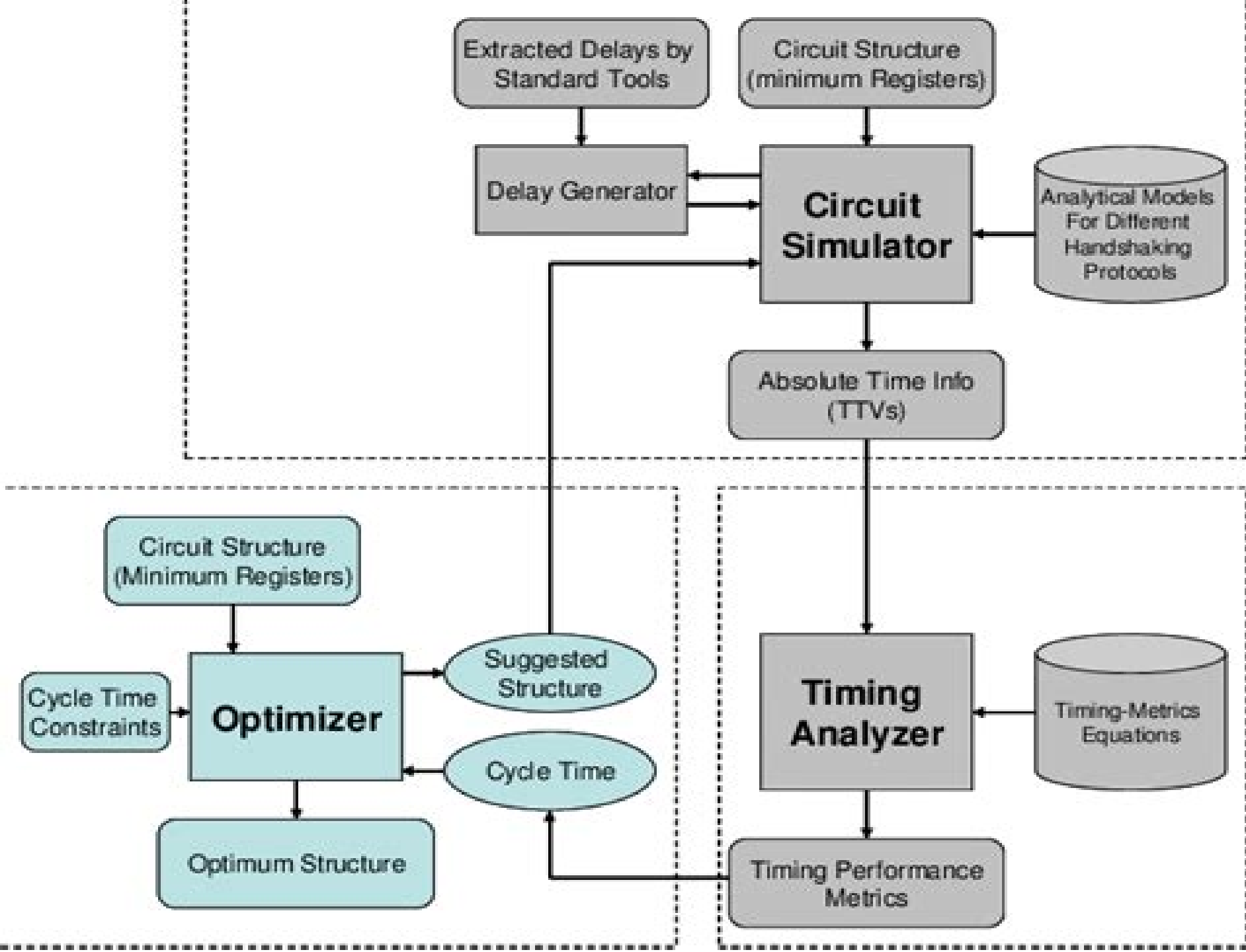




Performance Modeling Analysis And Optimization For Asynchronous Circuitsstatic And Statistical Analysis Approaches

Yijin Wang



Performance Modeling Analysis And Optimization For Asynchronous Circuitsstatic And Statistical Analysis Approaches:

Performance Modeling, Analysis and Optimization for Asynchronous Circuits:Static and Statistical Analysis Approaches Eslam Yahya,Marc Renaudin,Laurent Fesquet,2015-10-18 Asynchronous circuits provide efficient solutions for many of the recent nanometric technologies although the lack of analysis and optimization tools has limited the commercial spread of this technology This book helps readers to understand the difficulties of modeling and analyzing asynchronous circuits A new modeling methodology is introduced it is used to build Asynchronous Static Timing Analysis ASTA and Asynchronous Statistical Static Timing Analysis ASSTA These fast and accurate methods are used to optimize the circuit speed against its hardware size In addition the book investigates the handshaking protocol effect on different asynchronous circuit performance metrics speed power consumption EMI and robustness against process variability The book is accompanied by AHMOSE Asynchronous High speed Modeling and Optimization Tool set a demonstrative software which provides to the user a better understanding and usage of the explained methods Electrical & Electronics Abstracts ,1972 **Government Reports Announcements & Index** ,1994 *A General Approach to Performance Analysis and Optimization of Asynchronous Circuits* Tak Kwan Lee,Alain J. Martin,California Institute of Technology. Division of Engineering and Applied Science,1995 **Performance Analysis and Optimization of Asynchronous Circuits** California Institute of Technology. Computer Science Dept. (CITCS),Steven Morgan Burns,Alain J. Martin,1990 For a large class of asynchronous circuits including those produced by using our synthesis method these techniques produce the global optimum of the performance metric A CAD tool has been implemented to perform this optimization Performance Analysis and Optimization of Asynchronous Circuits Produced by Martin Synthesis California Institute of Technology. Computer Science Dept. (CITCS),Steven M. Burns,1990 Performance Modeling and Analysis of Asynchronous Pipelines for Designers Chih-ming Chang,1997 Better performance has been one of the main motivations behind the recent resurgence of interest in asynchronous circuits no matter whether this is always true or not We are particularly interested in the performance of pipelines since they are used extensively in current digital systems There exists an algorithm that can find the exact upper and lower bounds on the separation time of events in a certain class of process graphs However some transformations and complex mathematical analyses such as graph decomposition for infinite unfolded process graphs must be employed in order to reach exact bounds This algorithm may be a good candidate for the application of CAD tool development and circuit synthesis but it tends to block designers from visualizing what factors really affect the performance of asynchronous circuits In this thesis a simple approach is adopted to approximate the performance bounds Since our method is a symbolic approach instead of a numerical approach it allows designers to analyze the circuit performance while providing design guidelines and approaches at the same time Our approach has two steps First several basic modules are chosen including FIFO Fork Join

Toggle XOR Arbiter Call and Select XOR The individual output loop delay equivalent input delay and equivalent output delay are derived based on the Equal loopdelay theorem The result is a set of difference equations The performance approximation can be obtained with simple mathematical operations on the difference equations given the bounds of stagedelays That is the performance bounds of output loop delay equivalent input delay and equivalent output delay can be represented as the bounds of stagedelays Second for a larger system consisting of those basic modules its performance bounds can be derived directly from the bounds of output loop delay equivalent input delay and equivalent output delay of those basic modules which have been obtained already This approach allows a fast and easy calculation of performance bounds avoiding the need to rederive the difference equations for the whole system Both modular design and performance approximation are possible with our approach

Performance Analysis and Optimization of Asynchronous Circuits Steven M. Burns, 1991

Abstract Analytical techniques are developed to determine the performance of asynchronous digital circuits These techniques can be used to guide the designer during the synthesis of such a circuit leading to a high performance efficient implementation Optimization techniques are also developed that further improve this implementation by determining the optimal sizes of the low level devices CMOS transistors that compose the circuit

Performance Analysis and Optimization of Mixed Asynchronous Synchronous Systems J. Teich, 1994

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