

Formal Verification of Superscalar Microprocessors with Multicycle Functional Units, Exceptions, and Branch Prediction¹

Miroslav N. Velev^{*}

mvelev@ece.cmu.edu
<http://www.ece.cmu.edu/~mvelev>

Randal E. Bryant^{*, †}

candy.bryant@cs.cmu.edu
<http://www.cs.cmu.edu/~bryant>

^{*}Department of Electrical and Computer Engineering

[†]School of Computer Science

Carnegie Mellon University, Pittsburgh, PA 15213, U.S.A.

Abstract

We extend the Burch and Dill flushing technique [6] for formal verification of microprocessors to be applicable to designs where the functional units and memories have multicycle and possibly arbitrary latency. We also show ways to incorporate exceptions and branch prediction by exploiting the properties of the logic of Positive Equality with Uninterpreted Functions [4][5]. We study the modeling of the above features in different versions of dual-issue superscalar processors.

1 Introduction

In order for formal methods to scale for verification of modern microprocessors, they need to be applicable easily and with a high degree of automation to designs with multicycle functional units, multicycle memories, exceptions, and branch prediction. Burch and Dill's verification methodology has the potential to be highly automatic, but has previously been applied only to designs with single-cycle functional units and memories that produce their results instantaneously [5][6][7][21]. The approach is very elegant in using *flushing* of the processor—feeding it with bubbles until all instructions in flight complete their execution—in order to compute an abstraction function mapping Implementation states to a Specification state. (The difference between a bubble and a nop is that a bubble does not modify any user-visible state, while a nop increments the PC.) The correctness criterion is a commutative diagram, stating that an application of the transition function of the Implementation followed by flushing should produce the same user-visible state as first flushing the Implementation and then using the resultant user-visible state to apply the transition function of the Specification between 0 and k times, where k is the issue-width of the Implementation. As observed and exploited by Burch in his controlled flushing [7], we can change the logic during flushing, since the only purpose of that logic is to compute an abstraction function. Having an improper abstraction function will not compromise the verification and can only result in a false negative.

The same correctness criterion has been adopted by the theorem-proving community and applied to an out-of-order design with exceptions and interrupts by Sawada and Hunt [17] and to an out-of-order design with only arithmetic instructions by

Hosabettu, Srivas and Gopalakrishnan [13]. However, the former approach requires the user to manually build an intermediate abstraction of the processor and to define a large number of lemmas (Sawada defined nearly 4,000), necessary for the correctness proof. The latter approach requires the user to manually define a set of completion functions, one per unfinished instruction in flight, describing how that instruction will be completed, given that all the instructions that it has data dependencies on have already been completed. Furthermore, the user has to manually define a way to compose these completion functions in order to form the abstraction function for the processor. Both of these theorem-proving methods require months of manual work for complex designs, i.e., they are not automatic.

Not only has the Burch and Dill flushing technique not been applied to processors with multicycle functional units, but Hosabettu, Srivas and Gopalakrishnan [12] have claimed that it has the drawback of being hard to use for pipelines with indeterminate latency, particularly where an ALU computation might have a data-dependent duration or a memory hierarchy of multiple levels might have a non-deterministic delay.

In this work we extend Burch and Dill's flushing-based methodology to be applicable to microprocessors with functional units and memories of multicycle and possibly arbitrary latency. We also model exceptions and branch prediction. Our most complex designs have 10 abstract instruction types. They have two completely functional pipelines, each consisting of five stages, for a total of up to 10 instructions in flight. Therefore, exhaustive binary simulation must consider 10^{10} instruction sequences of 10 instructions each. Furthermore, accounting for possible data dependencies, raised exceptions, correctness/incorrectness of the branch predictions, and multicycle computations will make that number significantly higher. Even directed simulation will probably find it very hard, if at all possible, to generate all interesting instruction sequences for such a design. However, we were able to formally verify it in less than 44 minutes of CPU time.

2 Background

The key to our success is a very efficient decision procedure [21] for the logic of Equality with Uninterpreted Functions and Memories (EUFM) [6], which exploits the properties of Positive Equality [4][5] and the e_v encoding [10] to generate a propositional formula, which is then evaluated with BDDs [3] or SAT-checkers. We found BDDs to be unmatched by SAT-checkers and SVC [18] (a decision procedure for the logic of EUFM that does not exploit Positive Equality) when verifying correct designs. However, SAT-checkers outperform BDDs on buggy processors.

The syntax of EUFM [6] includes terms and formulas. A term can be an Uninterpreted Function (UF) applied on a list of argument terms, a domain variable, or an *ITE* operator selecting between two argument terms based on a controlling formula, such that *ITE(formula, term1, term2)* will evaluate to *term1* when *formula* = **true** and to *term2* when *formula* = **false**. A formula can be an Uninterpreted Predicate (UP) applied on a list of argu-

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Book Formal Verification Microprocessors Automatic Superscalar

Husam Saad Abu-Haimed



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Formal Verification of Microprocessors Miroslav Velev, 2015-02-04 Formal verification is the mathematical proof of correctness of computer systems Microprocessors are the most important components in computer systems and are increasingly being used in safety critical applications e.g. to monitor the health of patients to control the engines and breaks of cars to drive autonomous vehicles and fly autonomous aircraft and to control weapons systems As such the correctness of microprocessors is a matter of public safety and national security Furthermore for the companies that design and manufacture microprocessors or systems controlled by them the correctness of microprocessors is a matter of business success or failure Statistics from industrial microprocessor designs indicate that up to 90% of the engineering effort is spent on verification which increasingly becomes the bottleneck in developing new products Formal verification has the potential to significantly reduce the design time while also guaranteeing complete correctness However previous approaches for formal verification of microprocessors either do not scale for complex designs or require prohibitive amounts of manual effort by experts In contrast this book presents a highly automatic and scalable method for formal verification of complex processors including pipelined superscalar and VLIW designs

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Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference, 1995

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Formal Verification of VLIW Microprocessors with Speculative Execution Miroslav N. Velev, 2000 Abstract This is a study of the formal verification of a VLIW microprocessor that imitates the Intel Itanium 9 12 17 in features such as predicated execution register remapping advanced and speculative loads and branch prediction The formal verification is done with the Burch and Dill flushing technique 5 by exploiting the properties of Positive Equality 3 4 The contributions include an extensive use of conservative approximations in abstracting portions of the processor and a framework for decomposition of the Boolean evaluation of the correctness formula The conservative approximations are applied automatically when abstracting a memory whose forwarding logic is not affected by stalling conditions that preserve the correctness of the memory semantics for the same memory These techniques allow a reduction of more than a factor of 4 in the CPU time for the formal verification of the most complex processor model examined relative to the monolithic evaluation of the correctness formula for a version of the same processor where conservative approximations are not applied

Design and Verification of Microprocessor Systems for High-Assurance Applications David S. Hardin, 2010-03-02 Microprocessors increasingly control and monitor our most critical systems including automobiles airliners medical systems transportation grids and defense systems The relentless march of semiconductor process technology has given engineers exponentially

increasing transistor budgets at constant recurring cost This has encouraged increased functional integration onto a single die as well as increased architectural sophistication of the functional units themselves Additionally design cycle times are decreasing thus putting increased schedule pressure on engineers Not surprisingly this environment has led to a number of uncaught design flaws Traditional simulation based design verification has not kept up with the scale or pace of modern microprocessor system design Formal verification methods offer the promise of improved bug finding capability as well as the ability to establish functional correctness of a detailed design relative to a high level specification However widespread use of formal methods has had to await breakthroughs in automated reasoning integration with engineering design languages and processes scalability and usability This book presents several breakthrough design and verification techniques that allow these powerful formal methods to be employed in the real world of high assurance microprocessor system design

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